AMENDMENTS TO THE SPECIFICATIONS

Please delete paragraph [01] and insert the following amended paragraph [01]:

[01] This application is a continuation of U.S. Application Serial No. 10/176,843 filed June 21, 2002, which is a continuation-in-part of, and claims benefit of and priority from, U.S. Application Serial No. 10/100,757 filed March 19, 2002, titled "Synchronous Controlled, Self-timed Local SRAM Block", now U.S. Patent No. 6,646,954 issued November 11, 2003, which is a continuation-in-part of U.S. Application Serial No. 09/775,701, filed February 2, 2001, now U.S. Patent No. 6,411,557, issued June 25, 2002, the complete subject matter of each of which is incorporated herein by reference in ~~its~~ their entirety.

Please delete paragraph [230] and insert the following amended paragraph [230]:

[230] In one embodiment of the present invention, each block is selected by at least one line (or by predecoding a group lines) in the higher address predecoded line group. A higher address predecoder line shifts only if the shift pointer points to the particular ~~redecoder~~ predecoder line or the previous line has shifted.

Please delete the Abstract of the Disclosure and insert the following amended Abstract:

Abstract of the Disclosure

The present invention relates to a system and method for providing redundancy in a hierarchically memory, by replacing small blocks in such memory. The present invention provides such redundancy (i.e., replaces such small blocks) by either shifting predecoded lines or using a modified shifting predecoder circuit in the local predecoder block. In one embodiment, the hierarchal memory structure includes ~~at least one active predecoder of aadapted to be shifted out of use; and~~ at least one redundant predecoder adapted to be shifted in for at least one active predecoder of a plurality of predecoders adapted to be shifted out.